AF/1700

DOCKET NO. : HUGGINS-6

PATENT #14

da 6/13/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of::

Harold Huggins

Serial No.: 09/715,~~615~~ 651

Filed: November 17, 2000

For: METHOD FOR MAKING A RADIO FREQUENCY COMPONENT AND COMPONENT PRODUCTION THEREBY

Grp./A.U.: 1765

Examiner: Vinh, Lan

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF FIRST CLASS MAILING

I hereby certify that this correspondence, including the attachments listed, is being deposited as First Class Mail with the United States Postal Service, in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313-1450, on the date shown below.

5-1-2003 Elizabeth Schumacher
Date of Mailing Signature of person mailing

Mail Stop Appeal Brief - Patents

Sirs:

APPELLANT'S BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from a Final Rejection mailed December 4, 2002, of Claims 1, 4-5, 8-9, 11-14, 17, 20-24 and 26-28. The Appellants submit this Brief in triplicate as required by 37 C.F.R. §1.192(a), with the statutory fee of $320.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorize the Commissioner to charge any additional fees connected with this communication or credit any overpayment to the Deposit Account No. 08-2395.

This brief contains these items under the following headings, and in the order set forth below, in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF THE INVENTION

VI. ISSUES

VII. GROUPING OF CLAIMS

VIII. SUMMARY OF REFERENCES RELIED ON BY THE EXAMINER

IX. APPELLANTS' ARGUMENTS

X. APPENDIX - CLAIMS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems, Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

The Appellants originally submitted Claims 1-35 in the application. In response to an Office Action dated May 1, 2002, the Appellants elected to prosecute the invention of a method Group I, namely Claims 1-28. In response to a subsequent Office Action, the Appellants have amended Claims 1, 4, 10, 12-14, 23 and canceled Claims 2-3, 6-7, 10 and 15-16, 18-19 and 25 without prejudice or disclaimer. Accordingly, Claims 1, 4-5, 8-9, 11-14, 17, 20-24 and 26-28 currently stand rejected and no claims are objected to or allowed. Claims 1, 4-5, 8-9, 11-14, 17, 20-24 and 26-28 are being appealed.

IV. STATUS OF AMENDMENTS

On February 4, 2003, the Appellants filed a Request For Reconsideration in response to a Final Rejection mailed December 4, 2002. By advisory action mailed February 11, 2003, the Examiner notified the Appellants that the request did not place the application in condition for allowance.

V. SUMMARY OF THE INVENTION

The present invention is directed to a method for making a radiofrequency (RF) component (Claim 1). The method comprises forming a dielectric layer 11 on a semiconductor substrate 12 and forming and patterning a conductive layer 13 on the dielectric layer 11 to define the RF component (Illustration 1). The method further includes forming a plurality of openings 14 on opposing sides and through the RF component at least to the semiconductor substrate 12. The openings 14 have a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns. The method also includes releasing

the RF component from the semiconductor substrate 12 by exposing the semiconductor substrate 12 to a dry etchant comprising XeF_2 passing through the at least one opening 14 to the semiconductor substrate 12.

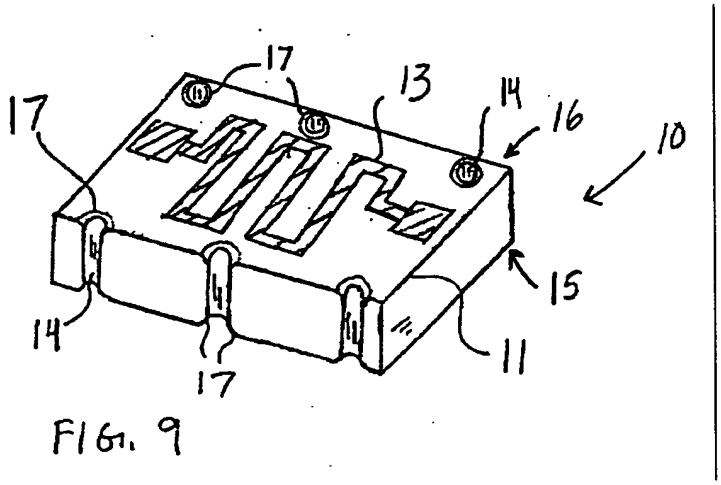


FIG. 9

Illustration 1

VI. ISSUES

A. First Issue Presented for Review:

Whether Claims 1, 4-5, 11-14, 17, 22-24 and 28 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,853,601 to Krishaswamy *et al.* ("Krishaswamy") in view of U.S. Patent No. 6,093,330 to Chong *et al.* ("Chong") and further in view of U.S. Patent No. 5,998,816 to Nakaki *et al.* ("Nakaki").

B. Second Issue Presented for Review:

Whether Claims 8, 20 and 26 are unpatentable under 35 U.S.C. §103(a) over Krishaswamy in view of Chong and further in view of Nakaki and further in view of U.S. Patent No. 6,131,256 to Dydyk *et al.* ("Dydyk 256").

C. Third Issue Presented for Review:

Whether Claims 9, 21 and 27 under 35 U.S.C. §103(a) as being unpatentable over Krishaswamy in view of Chong and further in view of Nakaki and further in view of U.S. Patent No. 5,424,698 to Dydyk *et al.* ("Dydyk 698")

VII. GROUPING OF CLAIMS

Claims 1, 4-5, 8-9, 11-14, 17, 20-24 and 26-28 stand or fall together.

VIII. SUMMARY OF REFERENCES RELIED ON BY THE EXAMINER

A. Krishaswamy

Krishaswamy. is directed to a top via etch technique for forming dielectric membranes for thin film devices (Abstract). Krishaswamy's FIGURE 5D (Illustration 2) presents a cross sectional view of a device exposed to a top-via etch technique where vias or windows 113 are formed through a dielectric member 103 and photoresist 111 to expose a substrate 101 near first and second opposing ends of a film bulk acoustic resonator (FBAR) comprising an input electrode 105, piezoelectric layer 107, and output electrode 109 (Column 3, Lines 55-60). An isotropic dry Reactive Ion Etch (RIE) using SF_6 is carried out through the windows 113 at 0.8 microns per minute for 125 minutes in 30 minute segments (FIGURE 5E and 5F) to form air gaps 115 in the substrate 101 such that the ends of the FBAR extend over the dielectric membrane 103 (Column 5, Line 61 to Column 6, Line 18).

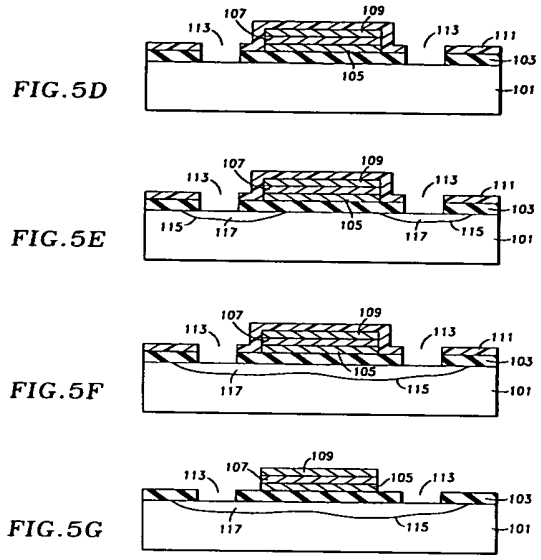


Illustration 2

Krishaswamy's etching procedure is specifically tailored to protect the photoresist 111 from polymerizing (Column 6, Lines 7-10). Krishaswamy specifically rejects etching through small openings because, among other things, Krishaswamy believed this to negatively impact reproducibility. (Column 3, Lines 45-53) Rather, the shape of the windows 113 used by Krishaswamy are depicted in FIGURE 6 (Illustration 3), a planar view of the device depicted in FIGURE 5G (Column 6, Lines 29-32), as long rectangular trenches that extend substantially the length of the substrate 101.

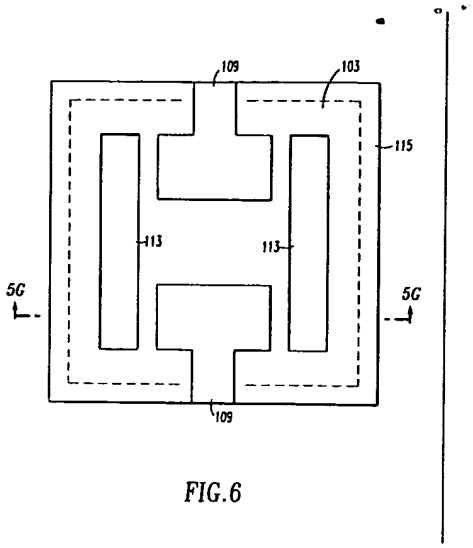


FIG.6

Illustration 3

B. Chong

Chong is directed to a process for making tunnels, cavities and similar subsurface structures within a substrate (Column 1, Lines 12-17). As illustrated in FIGURE 15 of Chong (Illustration 4) one or more patterned vias 86, 88 are formed in a mask layer 12 covering a substrate 10 and then an isotropic etch using SF_6 (Column 9, Line 66) is applied through the vias 86, 88 to form a cavity 104. (Column 11, Line 32 to Column 12, Line 10). Chong indicates that the mask pattern is transferred to the substrate (Column 9, Lines 34-40), and elsewhere remarks that multiple subsurface structures having any desired spacing, configuration and length can be provided by the via's location, spacing and length (Column 4, Lines 41-51). As illustrated in FIGURE 15 of Chong, a linear cavity 104 can be provided by etching through linear vias 86, 88.

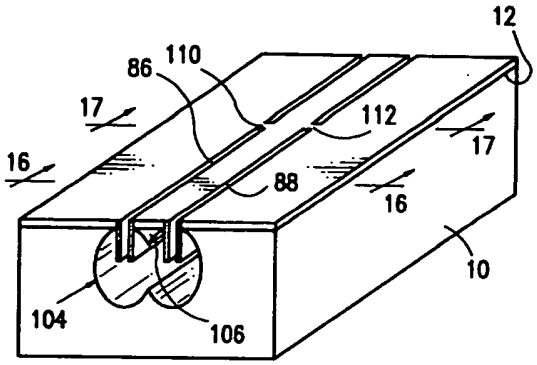


FIG. 15

Illustration 4

Or, as shown in FIGURE 44 (Illustration 5), a curved tunnel 430 is formed from a curved via.

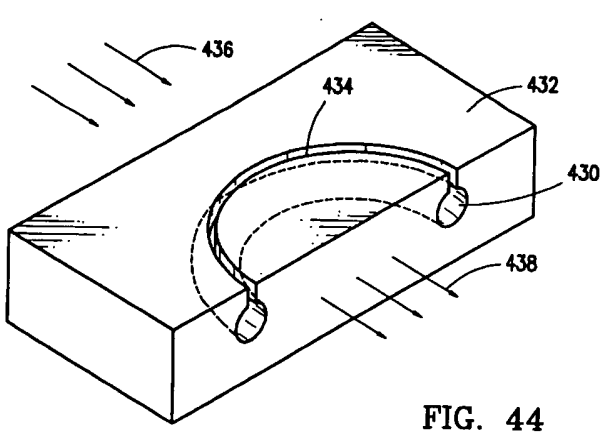


FIG. 44

Illustration 5

C. Nakaki

As illustrated in FIGURE 1A and 1B (Illustration 6), Nakaki is directed to a sensor element 3 interconnected to a semiconductor circuit 6 interconnect with a wire 4 (Column 4, Lines 7-58). A cavity 8 in the substrate 1 below the sensor 3 is formed by etching the substrate 1 through an L-shaped hole 2. The sensor 3 is supported on a film 4. Nakaki is concerned with undesired removal

of substrate in the (111) direction when performing anisotropic etching mainly in the (110) direction. (Column 1, Lines 36-48). To prevent this, Nakaki forms etchant resistant regions 7 to confine the size of the cavity 8 formed in the substrate. (Column 5, Lines 1-6). Nakaki's etchant is a fluoride of a rare gas such as xenon difluoride or kypton fluoride (Column 4, Lines 65-67).

FIG. 1A

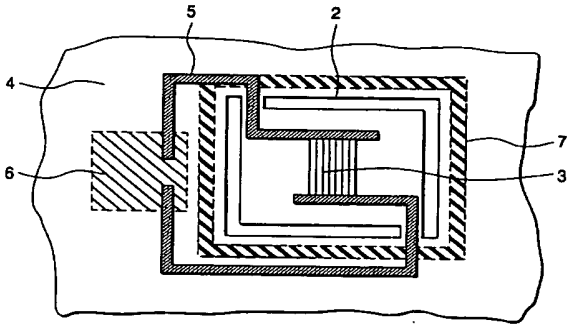


FIG. 1B

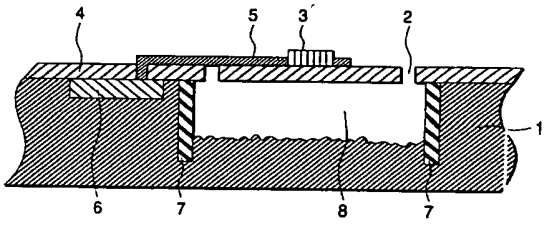


Illustration 6

D. Dydyk 256

Dydyk 256 is directed to a temperature compensated resonator having a substrate including a cavity produced by backside etching (Abstract; Column 4, Lines 54-58). The resonator may be made of low acoustic loss materials such as, Al and alloys thereof (Column 2, Lines 16-18).

E. Dydyk 698

Dydyk 698 is directed to a ferrite disk semiconductor resonator that interacts with interconnects when the ferrite disk is activated by a constant magnetic field (Abstract). An insulating material made of silicon oxide or silicon nitride is deposited on over the interconnects (Column 4, Lines 41-54).

IX. APPELLANT'S ARGUMENTS

The Appellants will now address the issues and grounds for rejection relied upon by the Examiner in the order set forth above.

A. First Issue

The Examiner rejected Claims 1, 4-5, 11-14, 17, 22-24 and 28 under 35 U.S.C. §103(a) as being unpatentable over the combination of Krishaswamy in view of Chong and further in view of Nakaki. Regarding Claim 1, the Examiner asserts that Krishaswamy teaches a dielectric layer 103 on a semiconductor substrate 101 and forming a patterned conductive layer 109 on the dielectric layer 103 to form an FBAR (Illustration 2). The Examiner further asserts that Krishaswamy discloses forming a plurality of vias 113 on opposites sides through the FBAR and dielectric layer 103 through to the substrate 101, and exposing the substrate to a dry fluorine etchant to form an air gap beneath the FBAR.

The Examiner admits that Krishaswamy does not disclose specific ranges between the opening and the diameter of the opening. For these elements, the Examiner uses Chong. The Examiner asserts that Chong general remark that multiple subsurface structures having any desired

spacing, configuration and length can be provided by the via's location, spacing and length (Column 4, Lines 41-51) means that one skilled in the art would find it obvious to modify Krishaswamy in view of Chong using routine experimentation to produce any desired range for the spacing and diameter of the claimed opening (Page 3, Line 10-13 of Examiner's Final Rejection, mailed December 4, 2002).

The Examiner further admits that the combination of Krishaswamy and Chong do not disclose that XeF_2 etchant gas is passed through the openings to the substrate. For this element, the Examiner uses Nakaki. The Examiner maintains that one skilled in the art would modify Krishaswamy and Chong by passing XeF_2 etchant gas through the openings because both Krishaswamy and Nakaki are concerned with exposing the semiconductor structure to fluorine etchant to remove the component from the substrate and Nakaki teaches that XeF_2 etchant gas can remove substrate below Nakaki's sensor element.

The Appellants respectfully disagree with the Examiner's grounds for rejecting Claim 1 and its dependent claims, as well as Claims 14 and 23 and their respective dependent claims.

First, the Appellants reiterate that the combination of Krishaswamy, Chong and Nakaki do not teach or suggest each element of the claimed invention, namely, forming a plurality of openings on opposing sides and through the RF component at least to the semiconductor substrate, the openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns. As noted in a previous Office Action response, Krishaswamy depicts forming two rectangular trenches (Illustration 3) and Nakaki depicts forming L-shaped trenches (Illustration 6), that extend substantially the length of the substrate. One embodiment of Chong similarly depicts two

rectangular via channels 86, 88 that extend substantially the length of the substrate (Illustration 4). Chong does not teach or suggest openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns, as recited in Claim 1.

The Appellants respectfully submit that Chang's general remark that multiple subsurface structures having any desired spacing, configuration and length can be provided by the via's location, spacing and length, would be interpreted by one skilled in the art as a general teaching that a trench of a particular desired shape can be made by forming a via of the same shape in substrate. This interpretation is supported by Chong's statement that in the embodiment presented in FIGURE 15 (Illustration 4), the mask pattern is transferred to the substrate (Column 9, Lines 34-40) and by presenting embodiments such as FIGURE 44 (Illustration 5) where a curved tunnel is formed using a curved via. This interpretation is further supported by Chong's desire to form microstructures in fluid flow applications (Column 4, Lines 1-12).

Moreover, Appellants maintain that there is no teaching or suggestion in the asserted combination of references that the claimed opening diameters and spacing are simply process variables easily arrived at by routine experimentation as suggested by the Examiner. To the contrary, Krishaswamy teaches a very controlled etching process with a isotropic dry Reactive Ion Etch (RIE) using SF_6 for a etch time of 125 minutes performed in segments to prevent the photoresist etch mask from polymerizing (Col. 3, lines 55-60, Col. 5, lines 59-67 and Col. 6, lines 1-10). Nakaki, to prevent the undesired removal of substrate in the (111) direction when performing anisotropic etching with XeF_2, forms etchant resistant regions to confine the size of the cavity formed in the substrate. (Column 5, Lines 1-6). The consideration that Krishaswamy and Nakaki place on their

etching protocols indicates that via openings and spacings are not just routine process variables when manufacturing the radio frequency (RF) component of the claimed inventions.

The Appellants, respectfully maintain that the combination of Krishaswamy, Chong and Nakaki to arrive at the claimed inventions requires the improper use of hindsight. *See Pentec, Inc. v. Graphic Controls Corp.*, 776 F.2d 309, 227 USPQ 766 (Fed. Cir. 1985) (prior art may not be gathered with the claimed invention in mind); *In re Fine*, 837 F.2d 1071. 5 USPQ2d 1596 (Fed. Cir. 1988) ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention"). Therefore, the combination of Krishaswamy, Chong and Nakaki fails to teach or suggest forming a plurality of openings on opposing sides and through the RF component at least to the semiconductor substrate, the openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns as recited in Claim 1 and its dependent Claims, as well as Claims 14 and 23 and their respective dependent claims.

In addition, the Appellants submit that the combination of Krishaswamy, Chong and Nakaki is improper because, as noted above, Krishaswamy teaches a very controlled process for conducting an isotropic dry Reactive Ion Etch (RIE) using SF_6 in segments to prevent the photoresist etch mask from polymerizing. One skilled in the art would not be motivated to modify Krishaswamy by attempting to implement Chong's general remark that multiple subsurface structures having any desired spacing, configuration and length can be provided by the via's location, spacing and length.

Additionally, as noted in a previous Office Action response, Nakaki, cited by the Examiner for the proposition of teaching an etchant XeF_2 gas is not properly combinable with Krishaswamy because undue experimentation would be necessary to arrive at conditions, if any, that would allow

etching of Krishaswamy's substrate without polymerizing Krishaswamy's photoresist. As noted above, Nakaki controls his anisotropic etching process with XeF_2 gas by forming etchant resistant regions 7 in the substrate. One skilled in the art would not be motivated to alter Krishaswamy's controlled etching procedure by etching with XeF_2 gas because Nakaki suggests that this process is difficult to control without the aid of etchant resistant regions 7 in the substrate.

Because the combination of Krishaswamy, Chong, and Nakaki does not teach or suggest all elements of independent Claims 1, 14 and 23 and are not properly combinable, they fail to establish a *prima facie* case of obviousness with respect to independent Claims 1, 14 and 23 and their respective dependent claims. Therefore, because Claims 1, 4-5, 11-14, 17, 22-24 and 28 are not obvious, the Appellants s respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection with respect to these claims under 35 U.S.C. §103(a).

B and C. Second and Third Issue

The Examiner rejected Claims 8, 20 and 26 under 35 U.S.C. §103(a) as unpatentable over the combination of Krishaswamy, Chong and Nakaki, further in view of Dydyk 256. The Examiner cited Dydyk 256 soley for the proposition of teaching a resonator/RF component having an electrode layer of aluminum. The Examiner similarly rejected Claims 9, 21 and 27 under 35 U.S.C. §103(a) as being unpatentable over the combination of Krishaswamy, Chong and Nakaki, further in view of Dydyk 698, where Dydyk 698 is cited only for the proposition of forming a insulating layer made of silicon oxide and silicon nitride. The Appellants respectfully disagree with the Examiner's grounds for rejecting these claims.

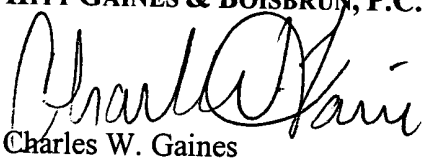
As discussed above, the combination of the Krishaswamy, Chong and Nakaki does not teach each element of the presently claimed invention and the combination of these reference is improper. Because neither Dydyk 256 nor Dydyk 698 cure the deficient teachings of this combination, this combination also fails to teach or suggest each and every element of the presently claimed inventions.

As such, the combined teachings of Krishaswamy, Chong and Nakaki and further in view of either Dydyk 256 or Dydyk 698, fail teach or suggest each and every element of independent Claims 1, 14 and 23 and their respective dependent claims, including Claims 8, 20 and 26 and Claims 9, 21 and 27. Therefore because these claims are not obvious, the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection with respect the Claims 8, 9, 20, 21, 26 and 27 under 35 U.S.C. §103(a).

For these reasons, the Appellants respectfully request the Board of Patent Appeals and Interferences to reverse the Examiner's Final Rejections with respect to Claims 1, 4-5, 8-9, 11-14, 17, 20-24 and 26-28.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.



Charles W. Gaines
Registration No. 36,804

Dated: 5/01/2003

HITT GAINES & BOISBRUN, P.C.
P.O. Box 832570
Richardson, Texas 75080
Tel: (972) 480-8800
Fax: (972) 480-8865

X. APPENDIX - CLAIMS

Claims 1-35 were originally filed in the Application. Claims 29-35 were subsequently withdrawn without prejudice or disclaimer in response to a restriction requirement. Claims 1, 4, 10, 12-14, and 23 were amended and Claims 2-3, 6-7, 10 and 15-16, 18-19 and 25 were canceled without prejudice or disclaimer. Claims 1, 4-5, 8-9, 11-14, 17, 20-24 and 26-28, the claims involved in this appeal, are as follows:

1. A method for making a radiofrequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming a plurality of openings on opposing sides and through the RF component at least to the semiconductor substrate, the openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor substrate to a dry etchant comprising XeF_2 passing through the at least one opening to the semiconductor substrate.

4. The method of Claim 1 wherein the openings are laterally adjacent portions of the conductive layer with no openings extending through the conductive layer.

5. The method of Claim 1 wherein forming the plurality of openings comprises forming the plurality of openings in a predetermined pattern.

8. The method of Claim 1 wherein the conductive layer comprises aluminum.

9. The method of Claim 1 wherein the dielectric layer comprises SiN.

11. The method of Claim 1 wherein the semiconductor substrate comprises silicon.

12. The method of Claim 1 where in the openings extend into the semiconductor substrate.

13. The method of Claim 1 wherein the openings substantially terminate at a surface of the semiconductor substrate.

14. A method for making a radio frequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming a plurality of openings on opposing sides and through the dielectric layer at least to the semiconductor substrate the openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor substrate to a dry etchant comprising XeF_2 passing through the openings to the semiconductor substrate.

17. The method of Claim 14 wherein forming the plurality of openings comprises forming the plurality of openings in a predetermined pattern.

20. The method of Claim 14 wherein the conductive layer comprises aluminum.

21. The method of Claim 14 wherein the dielectric layer comprises SiN.

22. The method of Claim 14 wherein the semiconductor substrate comprises silicon.

23. A method for making a radio frequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming a plurality of openings on opposing sides and through the dielectric layer in a predetermined pattern at least to the semiconductor substrate the openings having a diameter ranging from about 0.5 to about 20 microns and substantially uniform spacing between adjacent openings in a range of about 20 to about 200 microns; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor passing through substrate to a dry etchant comprising XeF2 passing the openings to the semiconductor substrate.

24. The method of Claim 23 wherein the predetermined pattern has substantially uniform spacing between adjacent openings.

26. The method of Claim 23 wherein the conductive layer comprises aluminum.

27. The method of Claim 23 wherein the dielectric layer comprises SiN.

28. The method of Claim 23 wherein the semiconductor substrate comprises silicon.